Multiport DDR Memory System IP

This is an advanced multiport DDR memory controller designed to simplify the task of handling multiple data streams in and out of a DDR SDRAM. This core is especially suited to video processing or other high rate data stream systems.

The specialized controller includes not only a DDR interface, but also a configurable state machine that can be setup to transfer data between FIFOs or buffer elements and the DDR device. Up to 16 write ports and 16 read ports are available.

Along with standard burst transfers, an advanced 2-D transfer mode is available. This allows for the very efficient reading and writing of image blocks within line organized image or video data without the need of internal FPGA ram based line buffers.

**Key Features**

- Large number of I/O ports
  - Up to 16 read ports
  - Up to 16 write ports
- 8, 16 or 32-bit DDR data bus width
- Multiple DDR technology support
  - CAS latency of 3
  - Mobile DDR
  - DDR1 / DDR2
- Up to 200MHz operation
- Programmable burst lengths
  - At run time
  - Fixed at configuration
  - Advanced 2-D burst
- Predictable performance
  - Simple formula to calculate number of cycles per port
  - Constant cycle mode : same cycles/port whether serviced or not
  - High efficiency mode: reduced cycles/port when not serviced
  - Known position of refresh
- High efficiency
  - Very low cycle overhead per port access
- Easy configuration
  - Windows command line utility
- Small
  - Only 250 Slices and one EBR in LatticeECP2/M

**Typical Usage**

- Optimized for LatticeECP2/M™ FPGAs
- Up to 16 IN ports and 16 OUT ports
- High DDR efficiency
- Easy to configure
- Mobile DDR, DDR1, DDR2 support
- 2-D transfers
Customer Interface

Applications
- Multimedia systems
- HDTV
- Video capture systems
- Video editing systems
- Scan rate converters
- Video synchronization
- Deinterlacing systems
- 2-D filters
- Picture in picture systems
- Multichannel data acquisition
- General purpose circular buffers
- Very deep FIFOs

Deliverables
- EDIF netlist
- RTL source code
- VHDL and Verilog test benches
- State machine generator tool
- Documentation

Other IP's
- VC-1 CODEC
- H.264 CODEC
- Video preprocessing core
- Motion estimation core
- Multiport DDR controller

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